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PATENT

S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Christopher J. Chevallier
Serial No.: 09/955,270
Filed: September 18, 2001
Title: SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT

Examiner: Unknown
Group Art Unit: Unknown
Docket: 703.019US3



## SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

When the above-referenced patent application is taken up for consideration, please amend the application as follows:

## IN THE CLAIMS

Please cancel claims 1, 6 and 15 without prejudice. Please enter new claims 22-77:

B-1 Cont

22. (New) A method of reducing a voltage, comprising:

applying the voltage to a transistor; and

providing the voltage reduced by a threshold voltage of the transistor at an output of the transistor, wherein the output of the transistor is coupled to a well that bounds the transistor.

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23. (New) The method of claim 22, wherein applying the voltage to the transistor comprises coupling the voltage to a first source/drain and a gate of the transistor.

Sub D1

24. (New) The method of claim 23, further comprising coupling the output of the transistor to a second source/drain of the transistor and to a semiconductor region in which the first and second source/drains are formed.

25. (New) The method of claim 24, wherein the first and second source/drains and the well are formed from a first type semiconductor material and the semiconductor region is formed from a second type semiconductor material.